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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/668,801	09/22/2000	Timothy J. Williams	0325.00417	2047

21363 7590 07/06/2005

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EXAMINER	
CAO, CHUN	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/668,801	WILLIAMS, TIMOTHY J.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-25 are remained and presented for examination in this application.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

4. Claims 1-3, 15-17, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Henson (Henson), US patent no. 6,158,014.

As per claim 1, Henson discloses an apparatus comprising:

a circuit [fig. 1] configured to generate an output having a frequency [clock speed of the deserializer, col. 3, lines 58-61] and adjust said frequency in response to a measured duration of a known time interval associated with a predefined bit pattern [8-bit/10-bit] occurring in an input data stream [col. 4, lines 9-14, 28-32, 58-67; col. 5, lines 44-53; col. 5, line 64-col. 6, line 11].

As per claim 2, inherently, Henson discloses that the input data stream comprises one or more of said time intervals [col. 4, line 58-col. 5, line 37].

As per claim 3, Henson discloses that time intervals are delimited by periodic events in said input data stream [col. 4, line 58-col. 5, line 37].

As per claim 15 is written in means plus function format and contains the same limitations as claim 1, therefore, the same rejection is applied.

As per claim 22, Henson discloses that predefined bit pattern comprises a packet identifier field of a SOF packet [col. 3, lines 35-55].

As per claim 23, Williams discloses that circuit comprises:

a detector circuit configured to generate a detection signal in response to detecting said predefined bit pattern in said input data stream [col. 3, lines 46-61; col. 4, lines 1-17]; and

a counter circuit configured to generate a count signal in response to said detection signal and said output [fig. 1; col. 4, lines 1-17].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-5 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henson (Henson), US patent no. 6,158,014 in view of Applicant Admitted Prior Art (AAPA).

As per claim 4, Henson does not disclose a start-of-frame (SOF) packets of a Universal Serial bus protocol.

AAPA discloses that periodic events comprise start-of-frame (SOF) packets [page 2, lines 16-17] of a Universal Serial bus protocol [page 2, lines 10-18].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Henson and AAPA, and the specific teaching of AAPA that would improve the functionality of Henson's system by implementing in USB protocol.

As per claim 5, inherently, AAPA teaches of adjusting the frequency within 0.25% of a host data rate [page 2, lines 15-18].

As per claim 25, inherently, AAPA discloses that input data stream comprises USB 2.0 host full-speed communications SOF packets [page 2, lines 10-18].

7. Claims 6-13, 18-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henson (Henson), US patent no. 6,158,014 in view of Jones (Jones), US patent no. 6,407,682.

As to claims 6 and 24, Henson discloses that the circuit comprises a calibration circuit configured to generate a control signal in response to said input data stream and said output [fig. 1; col. 4, lines 8-17].

Henson does not explicitly disclose an oscillator circuit.

Jones discloses a circuit [fig. 1] having an oscillator circuit [16, fig. 1] configured to generate said output in response to said control signal [fig. 1; col. 34-47].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Henson and Jones, and the specific teaching of Jones that would improve the functionality and integrity of Henson's system by implementing an oscillator circuit to provide clock signal.

As per claim 7, Jones discloses a digitally tunable oscillator circuit [16, fig. 1].

As to claims 8 and 9, Henson discloses a calibration circuit comprises a detector circuit configured to detect said predefined bit pattern and a SOF packet [col. 3, lines 46-61; col. 4, lines 1-17].

As to claims 10 and 12, inherently Henson discloses the calibration circuit comprises one or more counters that configured to count in response to said output [fig. 1; col. 4, lines 1-17].

As per claim 11, Henson discloses counters are configured to start counting in response to a first SOF packet and counting in response to a second SOF packet [col. 4, line 58-col. 5, lines 38].

As per claim 13, Henson discloses calibration circuit comprises a look-up table [col. 5, lines 1-32].

As per claim 14, Henson discloses the look-up table containing a number of values for adjusting frequency [col. 5, lines 1-32].

8. As to claims 16-21, claims 1-14 basically are the corresponding elements that are carried out the method of operating steps in claims 16-21. Accordingly, claims 16-21 are rejected for the same reason as set forth for claims 1-14.

9. Applicant's arguments filed 4/22/2005 have been fully considered but are not persuasive.

10. In the remarks, applicants argued in substance that 1) Henson does not appear to disclose or suggest a circuit configured to (i) generate an output having a frequency and (ii) adjust said frequency in response to a measured duration of a know time interval associated with a predefined bit pattern occurring in an input data stream.

11. The examiner respectfully traverses. Henson discloses that a circuit [fig. 1] configured to generate an output having a frequency [clock speed (clock speed is same

as clock rate for indicating a frequency) of the deserializer, col. 3, lines 58-61] and adjust said frequency in response to a measured duration of a known time interval associated with a predefined bit pattern [8-bit/10-bit] occurring in an input data stream [col. 4, lines 9-14, 28-32, 58-67; col. 5, lines 44-53; col. 5, line 64-col. 6, line 11]. In summary, Henson teaches of determining a data rate of a serial bitstream using pattern recognition and for matching a clock speed of a deserializer to that data rate. Therefore, Henson teaches the objects, features and advantages of the present invention including providing a method/an apparatus for adjusting a frequency of clock close/match to the input data rate.

Also see rejection above.

11. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chun Cao

June 30, 2005